

# PH3230

N-channel enhancement mode field-effect transistor

Rev. 03 — 25 June 2003

Product data

## 1. Description

The latest generation N-channel enhancement mode field-effect power transistor in a SOT669 (LFAK) package.

Product availability:

PH3230 in SOT669 (LFAK).

## 2. Features

- Logic level compatible
- Low drive current
- High density mounting
- Very low on-state resistance.

## 3. Applications

- DC-to-DC converters
- Computer motherboards
- Switched mode power supplies.

## 4. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBL286</p> <p><b>SOT669 (LFAK)</b></p>	<p>MBL288</p>
4	gate (g)		
mb	mounting base, connected to drain (d)		

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25\text{ °C}$	-	30	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}$	-	50	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	42	W
$T_j$	junction temperature		-	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	3.2	3.7	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	5.5	7.3	mΩ

## 6. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

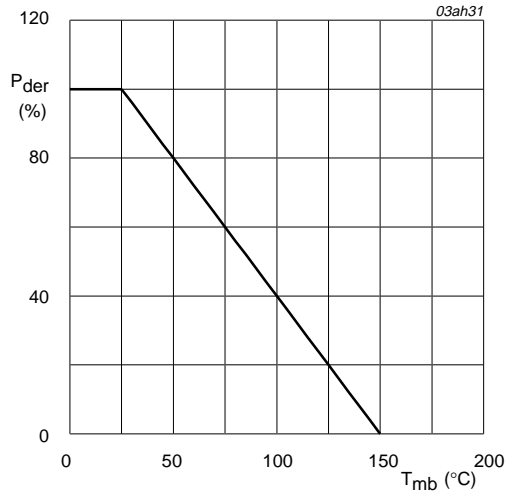
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage (DC)		-	±20	V
$I_D$	drain current (DC)	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$ ; <b>Figure 2 and 4</b>	-	50	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 4</b>	-	200	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <b>Figure 1</b>	-	42	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C

### Source-drain diode

$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	50	A
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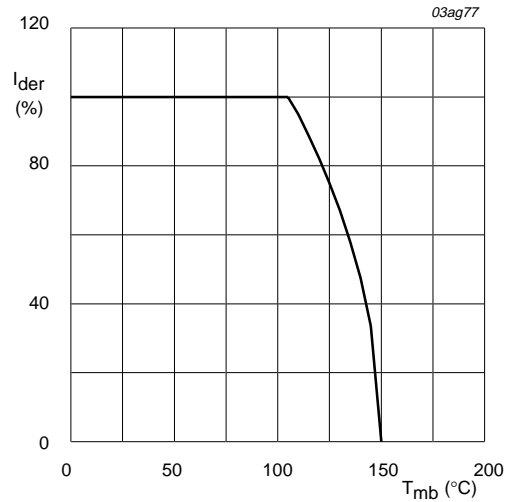
### Avalanche ruggedness

$I_{DS(AL)R}$	repetitive drain-source avalanche current	$T_j = 25\text{ °C}$	-	5	A
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	$T_j = 25\text{ °C}$ ; $R_{GS} \geq 50\text{ }\Omega$ ; $I_{DS(AL)R} = 5\text{ A}$ ; $V_{DD} = 15\text{ V}$ ; duty cycle < 0.1%; <b>Figure 3 and 16</b>	-	2.5	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

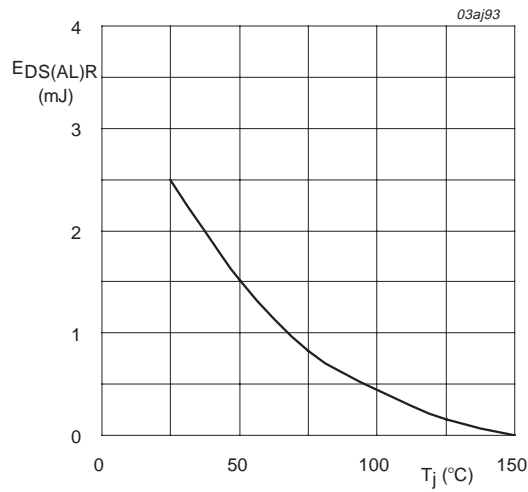
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



V<sub>GS</sub> ≥ 10 V

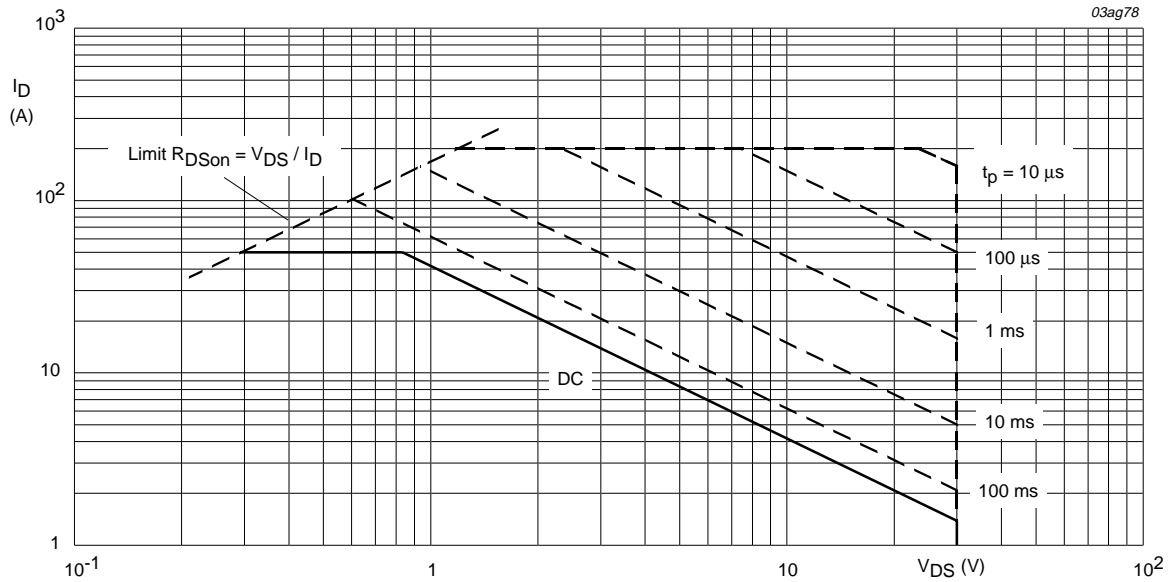
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**



I<sub>AR</sub> = 5 A; V<sub>DD</sub> = 15 V; duty cycle < 0.1%; R<sub>G</sub> ≥ 50 Ω

**Fig 3. Repetitive drain-source avalanche energy as a function of junction temperature.**



$T_{mb} = 25 \text{ }^\circ\text{C}$ ;  $I_{DM}$  is single pulse.

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 5	-	-	3	K/W

### 7.1 Transient thermal impedance

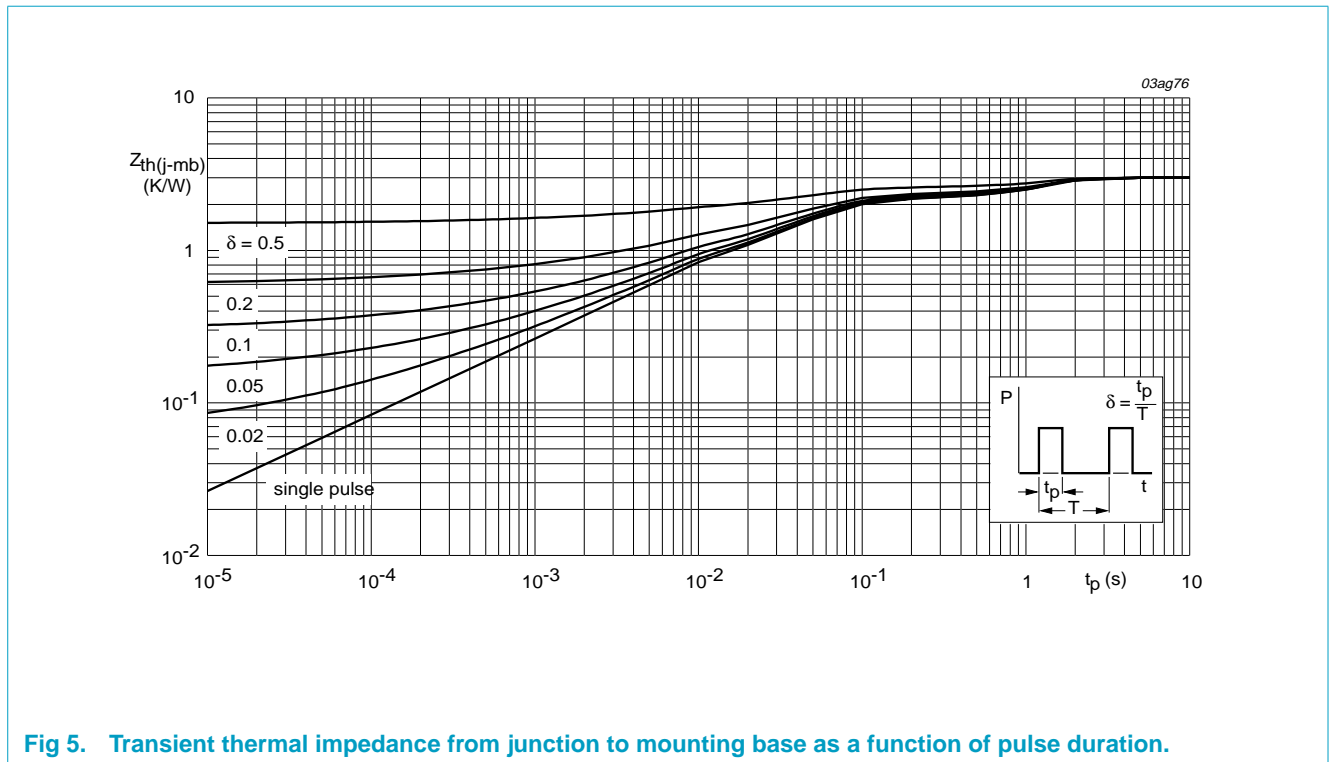


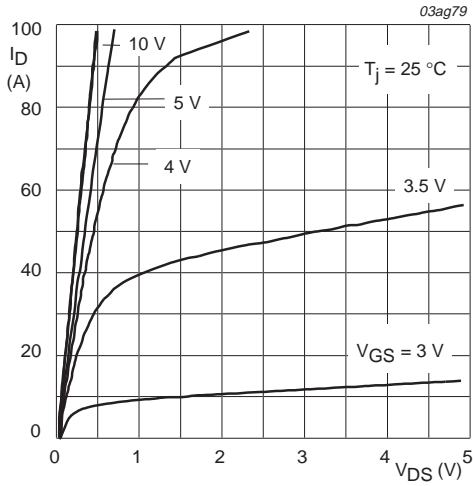
Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 8. Characteristics

**Table 5: Characteristics**

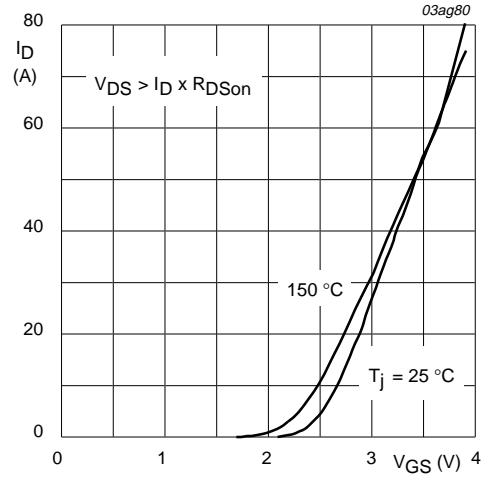
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ mA}; V_{GS} = 0\text{ V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$ ; <b>Figure 10</b>	1	1.9	2.5	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 16\text{ V}; V_{DS} = 0\text{ V}$	-	0.1	10	$\mu\text{A}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ ; <b>Figure 8 and 9</b>	-	3.2	3.7	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$ ; <b>Figure 9</b>	-	5.5	7.3	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 25\text{ A}$ ; <b>Figure 12</b>	39	55	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 50\text{ A}; V_{DD} = 10\text{ V}; V_{GS} = 10\text{ V}$ ; <b>Figure 15</b>	-	75	-	nC
$Q_{gs}$	gate-source charge		-	16	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	14	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$ ; <b>Figure 13</b>	-	4750	-	pF
$C_{oss}$	output capacitance		-	1160	-	pF
$C_{riss}$	reverse transfer capacitance		-	630	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}; I_D = 25\text{ A}; V_{GS} = 10\text{ V}; R_G = 4.7\ \Omega$	-	25	-	ns
$t_r$	rise time		-	50	-	ns
$t_{d(off)}$	turn-off delay time		-	90	-	ns
$t_f$	fall time		-	26	-	ns
<b>Source-drain (reverse) diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 50\text{ A}; V_{GS} = 0\text{ V}$ ; <b>Figure 14</b>	-	0.85	0.98	V
$t_{rr}$	reverse recovery time	$I_S = 50\text{ A}; dI_S/dt = -50\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}$	-	60	-	ns



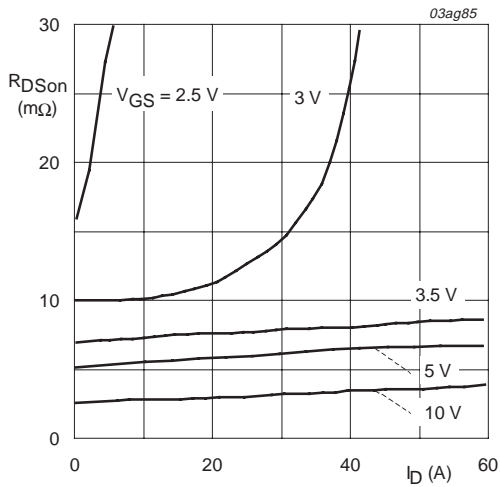
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



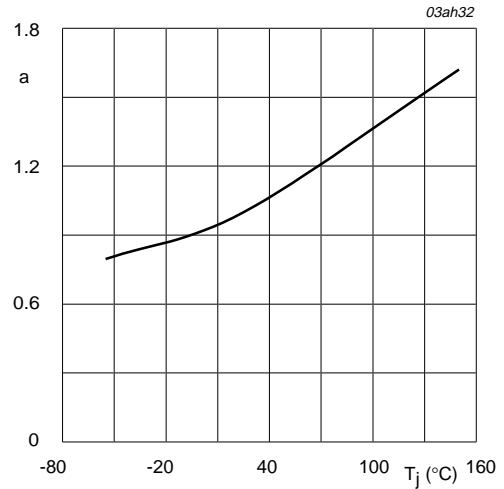
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



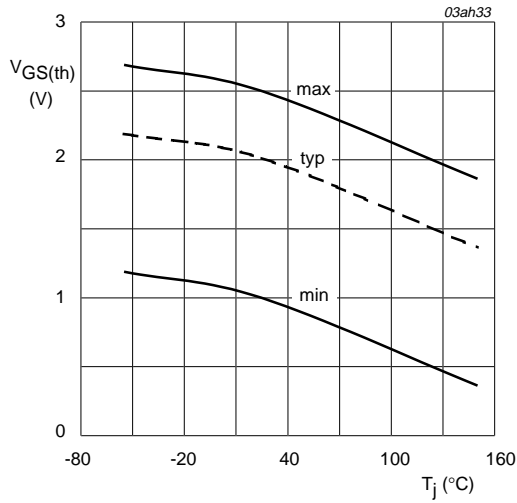
$T_j = 25\text{ }^\circ\text{C}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



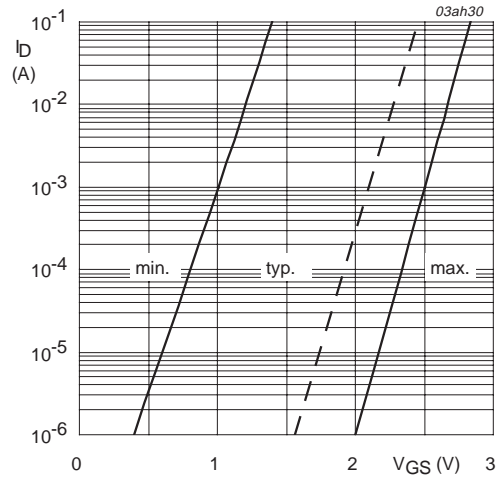
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.



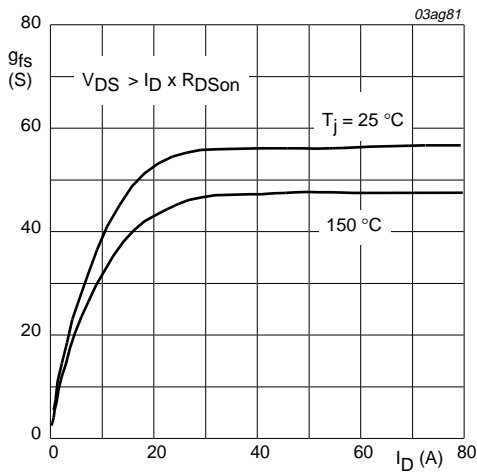
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



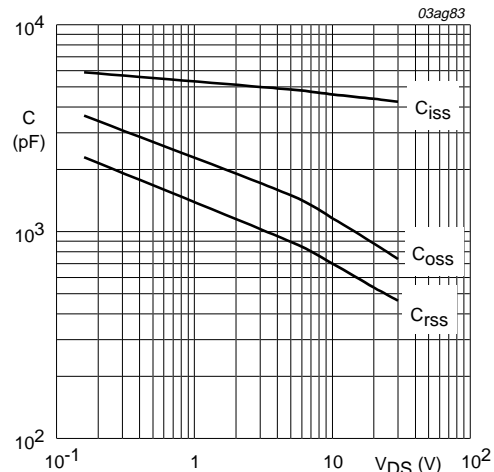
$T_j = 25 \text{ °C}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



$T_j = 25 \text{ °C}$  and  $150 \text{ °C}; V_{DS} > I_D \times R_{DS(on)}$

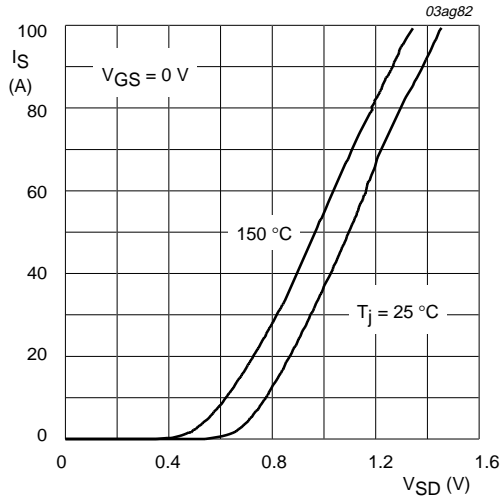
Fig 12. Forward transconductance as a function of drain current; typical values.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

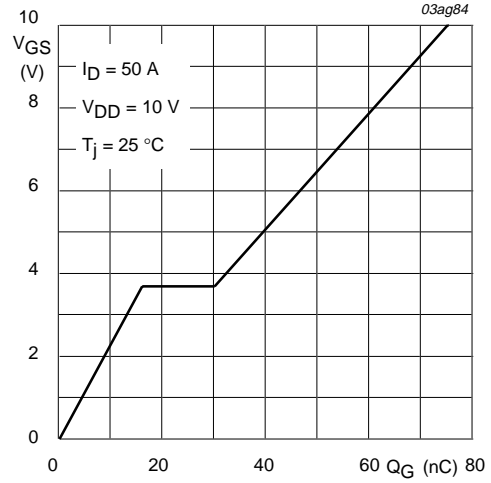
Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.





T<sub>j</sub> = 25 °C and 150 °C; V<sub>GS</sub> = 0 V

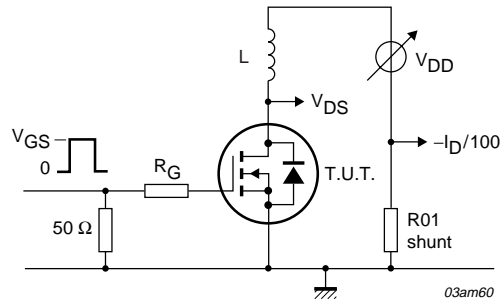
Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



T<sub>j</sub> = 25 °C; I<sub>D</sub> = 50 A; V<sub>DD</sub> = 10 V

Fig 15. Gate-source voltage as a function of gate charge; typical values.

## 9. Test information



$$E_{DS(AL)R} = 0.5 \times (LI_{DS(AL)R})^2 \times \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Fig 16. Avalanche energy test circuit.

10. Package outline

Plastic single-ended surface mounted package (Philips version LPAK); 4 leads

SOT669

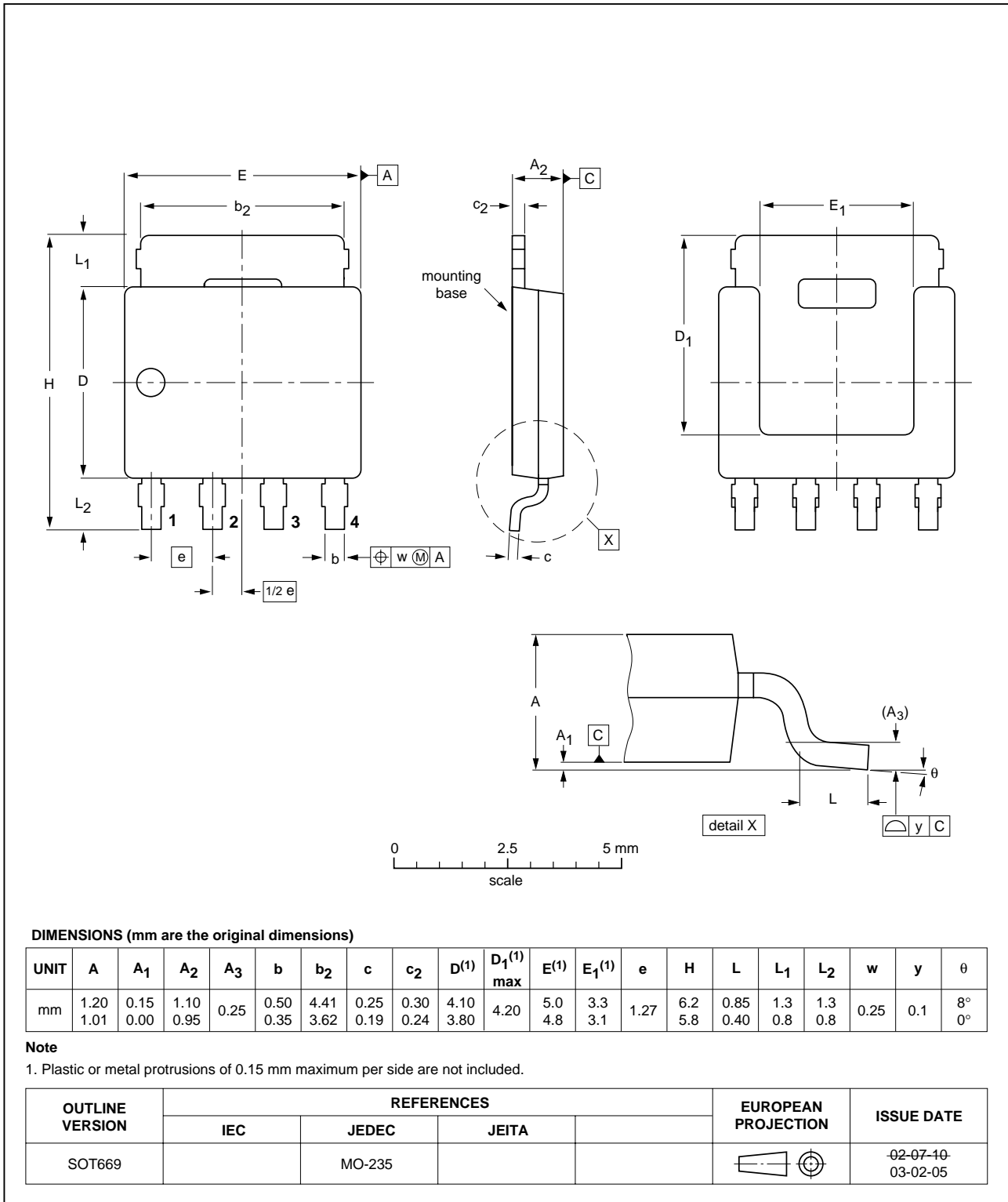


Fig 17. SOT669 (LPAK).

## 11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20030625	-	<b>Product Data (9397 750 10949)</b> Modifications: <ul style="list-style-type: none"><li>• JEDEC reference added to package outline drawing in <a href="#">Figure 17</a></li></ul>
02	20020905	-	<b>Product data (9397 750 10122)</b>
01	20020207	-	<b>Product data (9397 750 09395)</b>

## 12. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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